## AMENDMENTS TO THE CLAIMS

1-16. (canceled)

17. (currently amended) A method of forming a capacitor, comprising:

forming an in-laid conductor structure on a substrate, the in-laid conductor structure formed in an intra-layer dielectric;

forming an electrode layer directly on the conductor structure, wherein forming the electrode layer comprises forming columnar grains of an electrode layer material to be in direct contact with the conductor structure and selectively etching boundaries of the columnar grains;

forming a first layer over the electrode layer;

forming a second layer over the first layer;

forming a patterned masking layer over the second layer such that a portion of the second layer is exposed, and patterning the second, first and electrode layers in alignment with the masking layer, so as to form a vertical stack superjacent the conductor structure; and

forming a second conductor over the vertical stack.

18. (previously presented) The method of Claim 17, wherein the electrode layer comprises tantalum, the first layer comprises tantalum pentoxide, and the second layer comprises tantalum.

19. (original) The method of Claim 18, wherein the in-laid conductor and the second conductor comprise copper.

20. (currently amended) The method of Claim 17, wherein ~~forming the electrode layer comprises depositing~~ the columnar grains include tantalum.

21. (previously presented) The method of Claim 17, wherein forming the first layer comprises depositing tantalum pentoxide.

22. (previously presented) The method of Claim 21, wherein forming the second layer comprises depositing tantalum.

23. (previously presented) The method of Claim 17, further comprising forming an electrically insulating layer over the second layer and patterning the insulating layer so as to expose portions of the second layer prior to forming the second conductor.

24. (previously presented) The method of Claim 23, wherein forming a second conductor over the vertical stack includes making electrical contact between the second conductor and the second layer.

25-36. (canceled)

37. (currently amended) A method, comprising:

forming a first conductor structure in an inter-layer dielectric (ILD);

forming a bottom electrode layer directly on the first conductor structure, the bottom electrode layer consisting essentially of a material selected from the group consisting of tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), platinum (Pl), iridium (Ir) and ruthenium (Ru), wherein forming the bottom electrode layer comprises depositing a polycrystalline film of the material and selectively etching grain boundaries of the film with a wet chemical etch;

forming a dielectric layer directly on the bottom electrode layer;

forming a top electrode layer directly on the dielectric layer; and

forming a second conductor structure over the top electrode layer.

38. (canceled)

39. (canceled)

40. (previously presented) The method of claim 37, wherein the dielectric layer is barium strontium titinate (BST) or tantalum pentoxide ($Ta_2O_5$).

41. (previously presented) The method of claim 37, wherein the top electrode layer consists essentially of a material selected from the group consisting of Ru, TaN, TiN, WN, platinum (Pt) and iridium (Ir).

42. (previously presented) The method of claim 37, further comprising:

forming a hardmask layer over the top electrode layer;

forming a photoresist layer over the hardmask layer;

patterning the photoresist layer to expose a portion of the hardmask layer;

etching the exposed portion of the hardmask layer using a fluorine based etchant to expose a portion of the top electrode layer;

removing the photoresist layer by ashing; and

etching the exposed portion of the top electrode layer and the dielectric and bottom electrode layer directly under the exposed portion of the top electrode layer to form a capacitor

stack, wherein the second conductor structure is formed over the top electrode layer of the capacitor stack.

43. (previously presented) The method of claim 37, further comprising:

forming a nitride layer over the top electrode layer;

forming a second ILD over the nitride layer;

forming a via in the second ILD to expose a portion of the nitride layer;

etching the exposed portion of the nitride layer to expose a portion of the top electrode layer;

forming a conductive barrier layer over exposed surfaces of the via; and

filling the via with a conductive material to form the second conductor structure.

44. (currently amended) A method, comprising:

forming a first conductor structure in an inter-layer dielectric (ILD);

forming directly on the first conductor structure a bottom electrode layer to have a surface having a series of grooves ~~directly on the first conductor structure~~, the bottom electrode layer consisting of a layer of conductive material that substantially prevents diffusion of oxygen, oxygen-containing compounds and copper;

forming a dielectric layer directly on the bottom electrode layer;

forming a top electrode layer directly on the dielectric layer; and

forming a second conductor structure over the top electrode layer.

45. (canceled)

46. (previously presented) The method of claim 44, wherein the dielectric layer has a dielectric constant greater than that of silicon dioxide.

47. (previously presented) The method of claim 44, wherein the ILD is silicon dioxide, carbon doped oxides of silicon, fluorine doped oxides of silicon, porous oxides of silicon or organic polymers.

48. (previously presented) The method of claim 44, wherein the top electrode layer consists essentially of a material selected from the group consisting of Ru, TaN, TiN, WN, platinum (Pt) and iridium (Ir).

49. (previously presented) The method of claim 44, further comprising:

forming a photoresist layer over the top electrode layer;

patterning the photoresist layer to expose a portion of the top electrode layer;

etching through the exposed portion of the top electrode layer and the dielectric and bottom electrode layer directly under the exposed portion of the top electrode layer;

stripping the photoresist layer;

forming an etch stop layer over exposed surfaces of the ILD, bottom electrode layer, dielectric layer and top electrode layer;

forming a second ILD over the etch stop layer; and

forming the second conductor structure in the second ILD.

50. (new) The method of claim 44, wherein forming the bottom electrode layer having the surface having the series of grooves comprises:

depositing a polycrystalline film of the conductive material directly on the conductor structure; and

selectively etching grain boundaries of the film with a wet chemical etch.

51. (new) The method of claim 44, wherein forming the bottom electrode layer having the surface having the series of grooves comprises:

producing columnar grains of the conductive material directly on the conductor structure; and

selectively etching boundaries of the columnar grains.